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<u>L12</u>	L11 and (print\$4 or writ\$5 or transmi\$6)	170	<u>L12</u>
<u>L11</u>	L6 not 17	170	<u>L11</u>
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## Collections

### Definition, Editing, Browsing

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L7: Entry 190 of 196

File: DWPI

Mar 2, 1999

DERWENT-ACC-NO: 1999-224611

DERWENT-WEEK: 200022

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TITLE: Bit map data transmission mechanism for electrophotographic printer - includes printing data selection unit that outputs stored bit-map data when paper position sensor output corresponds with stored positional information

PATENT-ASSIGNEE:

ASSIGNEE

CODE

NEC CORP

NIDE

PRIORITY-DATA: 1997JP-0226498 (August 22, 1997)

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## PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
<input type="checkbox"/> <u>JP 11058876 A</u>	March 2, 1999		007	B41J021/16
<input type="checkbox"/> <u>JP 3029025 B2</u>	April 4, 2000		007	B41J021/16

## APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
JP 11058876A	August 22, 1997	1997JP-0226498	
JP 3029025B2	August 22, 1997	1997JP-0226498	
JP 3029025B2		JP 11058876	Previous Publ.

INT-CL (IPC): B41 J 21/00; B41 J 21/16; B41 J 29/50; G06 F 3/12

ABSTRACTED-PUB-NO: JP 11058876A

## BASIC-ABSTRACT:

NOVELTY - A sensor (4) detects pre-recorded ruled line or edge of paper. A printing position comparator compares the area designated by positional information stored in DRAM (2) and the output of the sensor. Based on the comparison result, a printing data selection unit outputs appropriate bit map data to the printer (3).

USE - For electrophotographic printer.

ADVANTAGE - Stores bit-map data in such a way that memory space is economized. Maintains exact printing position. DESCRIPTION OF DRAWING(S) - The drawing is a block diagram of the printer. (2) DRAM; (3) Printer; (4) Sensor.

CHOSEN-DRAWING: Dwg.1/6

TITLE-TERMS: BIT MAP DATA TRANSMISSION MECHANISM ELECTROPHOTOGRAPHIC PRINT PRINT  
DATA SELECT UNIT OUTPUT STORAGE BIT MAP DATA PAPER POSITION SENSE OUTPUT CORRESPOND  
STORAGE POSITION INFORMATION

DERWENT-CLASS: P75 T01 T04

EPI-CODES: T01-C05A; T04-G04; T04-G10A;

SECONDARY-ACC-NO:

Non-CPI Secondary Accession Numbers: N1999-166985

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L7: Entry 6 of 196

File: USPT

Dec 30, 2003

DOCUMENT-IDENTIFIER: US 6671257 B1

**\*\* See image for Certificate of Correction \*\***

TITLE: Feedback control method and device in ATM switching system

Abstract Text (1):

In an ATM switching system, an ABR service is implemented with a specific ABR control capability. A subscriber line processing device includes calculating a turnaround delay time of a cell, based on a period during which the cell doubles back at a terminal. A switch or a demultiplexer capable of detecting congestion. A rate calculator calculates a transmission rate corresponding to an output channel, and writes the calculated rate to the cell. A rate changer changes the transmission rate according to congestion. The rate changer counts the number of communicating connections. Then the number of communicating connections which should exist in a certain predetermined period is estimated based on the counted number of communicating connections. A coefficient is determined based on the estimated number of communicating connections and an actual number of communicating connections, and a next estimated value is estimated using the coefficient.

Application Filing Date (1):

20000710

Brief Summary Text (12):

An ATM switch in an ATM network notifies information about the network to a transmitting terminal by writing resource information (band information and congestion information) about the condition of the switch to an RM cell passing through the switch. The transmitting terminal which receives the RM cell to which the band and congestion information, etc. are written, recalculates its ACR (Allowed Cell Rate) according to the information, and makes a communication at a rate equal to or lower than the ACR.

Brief Summary Text (26):

A switch in the ER mode calculates a rate at which terminals can perform a transmission based on a congested state, and an available band in the switch, also calculates the explicit rate ER which is a rate at which a transmitting terminal is allowed to perform a transmission, and writes that ER to the ER field of an RM cell passing through the ATM switch in a forward direction (from the transmitting side to the receiving side), or in a backward direction (from the receiving side to the transmitting side). With these operations, the ATM switch can directly instruct the terminals of the rate, thereby performing rate control more precisely.

Brief Summary Text (27):

Furthermore, the switch itself can generate an RM cell, and transmit the generated RM cell to the transmitting terminal in addition to an RM cell transmitted from a terminal, regardless of the EFCI mode or the ER mode. At this time, the ATM switch can set the CI bit in the RM cell, or write a calculated explicit rate ER to the generated RM cell, depending on its congested state or available band.

Brief Summary Text (31):

Under the UPC control, a switch cannot change the monitoring rate immediately after it writes an ER or congestion indication to an RM cell. This is because a delay is

caused due to a time required for the following operations: the RM cell reaching a transmitting terminal; the transmitting terminal changing the ACR depending on the contents of the received RM cell; and the cell transmitted after that reaching the ATM switch. Therefore, the monitoring rate must be changed after a turnaround delay time elapses. The ATM switch making the ABR communication therefore needs to measure a delay time required for the UPC.

Brief Summary Text (32):

In the ABR communication, the monitoring rate must be changed after the ER written to the RM cell is changed according to the monitoring rate in the UNI, and the above described amount of delay time elapses.

Brief Summary Text (54):

An ABR controlling system according to the present invention is a system for notifying an allowed transmission rate of a transmitting terminal in an ATM network, as shown later in FIG. 7. The system comprises a shared buffer memory for temporarily storing cells transmitted from a transmitting terminal; an allowed transmission rate calculating unit for calculating the allowed transmission rate in correspondence with an output channel; an address management FIFO buffer memory for managing addresses of cells stored in said shared buffer memory; a congestion detection controlling unit for detecting congestion based on an amount of storage of the address management FIFO buffer memory or the shared buffer memory; and ER writing unit for writing the allowed transmission rate received from the allowed transmission rate calculating unit as it is, or a value obtained by lowering the allowed transmission rate according to a congestion notification signal received from the congestion detection controlling unit, to an RM cell, in order to notify the allowed transmission rate to the transmitting terminal, wherein the allowed transmission rate calculating unit obtains a number of active connections in which one or more cells arrive during an observation period, for each output channel, and calculates the allowed transmission rate by dividing the band of the output channel by the obtained number.

Brief Summary Text (55):

The allowed transmission rate calculating unit may comprise an arrived cell number counter for counting a number of arrived cells in correspondence with an output channel, and designating an observation period when the counted number reaches a predetermined number; an active VC (virtual connection) table to which a connection identifier of an arrived cell, which corresponds to the output channel, is written; an active VC number counter for obtaining the number of active VCs by counting the connection identifier which corresponds to the output channel, and is written to the active VC table; and an allowed transmission rate calculation controlling unit for calculating the allowed transmission rate by dividing the band of the output channel by the number of active VCs counted by the active VC number counter which corresponds to the output channel for which the arrived cell number counter counts the predetermined number of cells.

Brief Summary Text (57):

The ER writing unit may comprise an ER change parameter table in which a plurality of threshold values corresponding to the amount of storage of the address management FIFO buffer memory or said shared buffer memory, and decreasing coefficients corresponding to the plurality of threshold values, are set; and an ER calculating unit for multiplying the allowed transmission rate from said allowed transmission rate calculating unit, by the decreasing coefficient read from said ER change parameter table, based on information conveying that the amount of storage of said address management FIFO buffer memory or said shared buffer memory exceeds the plurality of threshold value.

Drawing Description Text (19):

FIG. 18 is a schematic diagram explaining an ER writing unit according to the present invention;

Detailed Description Text (12):

In FIG. 3, the same portions as those shown in FIG. 2 are denoted by the same reference numerals. 11 indicates a forward RM cell detecting/parameter extracting unit for an RM cell flowing in a forward direction (a forward RM cell hereinafter referred to as an F-RM cell). 12 indicates a controlling unit. 13 indicates a parameter storing memory. 14 indicates a backward RM cell detecting/parameter extracting unit for an RM cell flowing in a backward direction (a backward RM cell hereinafter referred to as a B-RM cell). 15 indicates a delay time calculating unit. 16 indicates a UPC parameter calculation/write controlling unit. 17 indicates a measured delay time storing memory.

Detailed Description Text (16):

(c) The controlling unit 12 writes the extracted connection identifier, sequence number SN, and the arrival time Ta, to the parameter storing memory 13.

Detailed Description Text (19):

(f) The UPC parameter calculation/write controlling unit 16 obtains the delay parameters  $\tau_{sub.2}$  and  $\tau_{sub.3}$  used under a UPC.

Detailed Description Text (23):

With the first method, the delay time T is measured an N (arbitrary integer number) number of times for a certain connection, and the maximum and minimum values among the measured values are respectively set as  $\tau_{sub.2}$  and  $\tau_{sub.3}$ . In this case, the UPC parameter calculation/write controlling unit 16 stores measured delay times Ts in the measured delay time storing memory 17, and determines the maximum and minimum values  $\tau_{sub.2}$  and  $\tau_{sub.3}$  among stored N delay times Ts when the delay time T is measured the N number of times.

Detailed Description Text (25):

With the second method, the delay time T is measured only once, and the delay parameters  $\tau_{sub.2}$  and  $\tau_{sub.3}$  are determined based on the measured delay time T. In this case, the UPC parameter calculation/write controlling unit 16 serves as a unit for calculating an exponential distribution curve in which the measured delay time T is used as its average, and determines the maximum and minimum values of the delay parameters based on the exponential distribution curve.

Detailed Description Text (27):

FIG. 7 is a schematic diagram showing the basic configuration of an ABR controlling system according to the present invention. This ABR controlling system comprises a shared buffer memory 21, allowed transmission rate calculating unit (or an explicit rate ER calculating unit) 22, ER writing unit 23, congestion detection controlling unit 24, and address management FIFO buffer memories 25-1 through 25-n. This ABR controlling system corresponds to the main portion of an ATM switch operating in an ER mode. It comprises "n" input channels (channels on an input side) and "n" output channels (channels on an output side).

Detailed Description Text (29):

One of the address management FIFO buffer memories 25-1 through 25-n, corresponding to the output channel identified by the VPI/VCI of the arrived cell, stores an address to which the arrived cell is written in the shared buffer memory 21. If the number of addresses stored in any of the address management FIFO buffer memories 25-1 through 25-n, which corresponds to a certain output channel, exceeds a predetermined number, it is determined that congestion occurs in that output channel. Then, a congestion detection signal is transmitted to the congestion detection controlling unit 24, which then outputs a congestion notification signal to the ER writing unit 23. In this case, the congestion detection controlling unit 24 can also detect an occurrence of congestion based on the amount of stored cells in the shared buffer memory 21.

Detailed Description Text (30):

The allowed transmission rate calculating unit 22 calculates an allowed transmission rate based on a band available for an ABR communication corresponding to each output channel. In this case, it calculates the allowed transmission rate regardless of whether or not congestion occurs. In a non-congested state, however, an allowed transmission rate corresponding to an output channel is transferred to the ER writing unit 23, and written to the explicit cell rate ER fields for forward and backward RM cells (F-RM and B-RM cells).

Detailed Description Text (31):

When the congestion notification signal is transmitted from the congestion detection controlling unit 24 to the ER writing unit 23, the ER writing unit 23 lowers the allowed transmission rate calculated in the allowed transmission rate calculating unit 22 according to a predetermined rule, and writes the lowered value to the explicit cell rate ER field of the received RM cell. The transmitting terminal receives the RM cell, and lowers its transmission rate according to the allowed transmission rate written to the explicit rate ER field of the received RM cell. With this process, the channel can be restored quickly from the congested state.

Detailed Description Text (35):

Assuming that an output channel to which an arrived cell is transmitted is #1, the connection identifier of that cell is written to the table for the output channel #1, and its cell arrival identification flag is set. Then, a counter in the arrived cell number counter 32 corresponding to the output channel #1 is incremented. In the meantime, the active VC number counter 34 counts a cell arrival identification flag for each output channel, and increments its value.

Detailed Description Text (37):

Accordingly, the value of the active VC number counter 34 indicates the number of connections in which user cells have arrived at least once until it is reset by a reset signal, that is, the number of active connections. It may be controlled that the active VC number counter 34 counts a newly written connection identifier, increments its value, sets the cell arrival identification flag in the active VC table 33, which indicates the increment, and counts no more connection identifiers whose cell arrival identification flag has already set in the table.

Detailed Description Text (38):

When receiving an observation period termination notification signal corresponding to an output channel from the arrived cell number counter 32, the allowed transmission rate calculation controlling unit 35 reads the number of active VCs from the active VC number counter 34 for each output channel, and transfers an allowed transmission rate for an output channel to the ER writing unit 23. The allowed transmission rate calculation controlling unit 35 outputs a reset signal to the arrived cell number counter 32, active VC table 33, and the active VC number counter 34, in order to respectively reset the number of arrived cells, connection identifier, cell arrival identification flag, and the number of active VCs.

Detailed Description Text (41):

Then, an allowed transmission rate  $Ba(n)$  is calculated based on an equation  $Ba(n) = B(n)/Nvc(n)$  (step S2). Note that  $B(n)$  indicates a band of each output channel. The allowed transmission rate  $Ba(n)$  is transferred to the ER writing unit 32 (step S3), and written to the field of the explicit cell rate ER for forward and backward RM cells. Here, the value obtained by dividing the band  $B(n)$  by the number of active VCs is defined as the allowed transmission rate  $Ba(n)$ . If the number of active VCs is large in this case, the allowed transmission rate  $Ba(n)$  becomes lower. As a result, an occurrence of congestion can be prevented.

Detailed Description Text (43):

In this embodiment, the number of active VCs  $Nvc(n)$  for each output channel in a predetermined observation period is counted (step S11). Then, the allowed transmission rate  $Ba(n)$  is calculated by using an arithmetic operation similar to that performed in the above described step S2 (step S12). The calculated transmission rate  $Ba(n)$  is transferred to the ER writing unit 32 (step S13). The predetermined observation period in this case is implemented by using the arrived cell number counter 32 shown in FIG. 8 as a timer for each output channel, or a common timer, and providing an observation period termination notification signal to the allowed transmission rate calculation controlling unit 35 at predetermined time intervals. With this process, the allowed transmission rate  $Ba(n)$  can be obtained in a similar manner as in the first embodiment.

Detailed Description Text (46):

The cell extracting unit 41 extracts a connection identifier of a cell transmitted from a transmitting terminal, and the arrived cell number counter 42 counts that cell for a corresponding output channel and increments its value. When the number of counted cells reaches a predetermined number, the arrived cell number counter 42 outputs an observation period termination notification signal to the allowed transmission rate calculation controlling unit 45. The active VC table 43 determines whether or not the connection identifier corresponding to the output channel was previously written. If NO, the connection identifier is written, and at the same time, the cell arrival identification flag is set. The active VC number counter 44 counts a connection identifier whose cell arrival identifier flag is set, and increments its value.

Detailed Description Text (49):

The active VC table 43 includes tables for output channels #1 through #n corresponding to the respective output channels, as shown in this figure. Each of the tables includes a connection identifier field CI, cell arrival identification flag field CF, and an MCR addition identification flag field AF. After the allowed transmission rate calculation controlling unit 45 calculates an allowed transmission rate for each output channel, it resets a corresponding table for an output channel. Then, it writes the connection identifier of the next arrived cell to the field CI, and sets the cell arrival identification flag in a corresponding field CF. Additionally, the allowed transmission rate calculation controlling unit 45 sets the MCR addition identification flag in the field AF, in order to indicate that an MCR corresponding to a referenced connection was previously added if reference is made to the active VC table 43 by the total MCR calculation controlling unit 47.

Detailed Description Text (56):

Then, the allowed transmission rate  $Ba(n)$  is calculated based on  $Ba(n) = MCR + [(B(n) - EMCR) / Nvc(n)]$  (step S25), and transferred to the ER writing unit. Note that the MCR is the minimum cell rate declared when a connection is established, and  $B(n)$  is a band of an output channel. With the above described process, an allowed transmission rate which can ensure the MCR for a transmitting terminal corresponding to an active VC, can be instructed.

Detailed Description Text (59):

FIG. 16 is a schematic diagram showing the second embodiment of the ABR controlling system according to the present invention. As shown in this figure, this ABR controlling system comprises a shared buffer memory 51, allowed transmission rate calculating unit 52, ER writing unit 53, congestion detection controlling unit 54, address management FIFO buffer memories 55-1 through 55-n which correspond to respective output channels, and congestion detecting units 56-1 through 56-n which correspond to the respective output channels.

Detailed Description Text (62):

If the number of addresses of cells in the shared buffer memory 51, which are stored in an address management FIFO buffer memory corresponding to a certain

output channel, exceeds a predetermined address management threshold value TH<sub>m</sub>, it is determined that congestion occurs in that output channel. Then, the congestion detection signal is provided to the congestion detection controlling unit 54. The congestion detection controlling unit 54 outputs the information about which address management threshold value the number of addresses stored in the address management FIFO buffer memory corresponding to the output channel exceeds, to the ER writing unit 53 as a congestion notification signal.

Detailed Description Text (63):

The allowed transmission rate calculating unit 52 behaves in a similar manner as the above described allowed transmission rate calculating unit 22 shown in FIG. 7. That is, it calculates an allowed transmission rate corresponding to a connection, and outputs the calculated rate to the ER writing unit 53. If there is no congestion notification signal from the congestion detection controlling unit 54 at this time, the allowed transmission rate is written to explicit cell rate ER fields of forward and backward RM cells in the connection, and the cells are transmitted.

Detailed Description Text (66):

Additionally, decreasing coefficients .alpha.1 through .alpha.m, with which the allowed transmission rate Ba is multiplied, are set on the condition that the number of stored addresses exceeds each of the threshold values TH1 through TH<sub>m</sub>, for the address management FIFO buffer memory 55. The decreasing coefficients .alpha.1 through .alpha.m are set in correspondence with the respective address management threshold values TH1 through TH<sub>m</sub>. If the number of stored address exceeds any of the address management threshold values TH1 through TH<sub>m</sub>, any of the decreasing coefficients .alpha.1 through .alpha.m, which corresponds to that value, is output. The ER writing unit 53 (refer to FIG. 16) multiplies the allowed transmission rate Ba output from the allowed transmission rate calculating unit 52, by any of the decreasing coefficients .alpha.1 through .alpha.m ( $1 < .alpha.1 < .alpha.2 < \dots < .alpha.m$ ) input via the congestion detection controlling unit 54, and writes the resultant value to the ER fields of forward and backward RM cells as the allowed transmission rate. With the above described process, the allowed transmission rate written to the ER fields of the RM cells can be lowered to a rate which prevents an occurrence of congestion.

Detailed Description Text (70):

FIG. 18 is a schematic diagram explaining the ER writing unit 53.

Detailed Description Text (71):

As shown in this figure, the ER writing unit 53 comprises an ER write controlling unit 61, ER calculating unit 62, and an ER change parameter table 63. The ER change parameter table 63 includes, for example, the address management threshold values TH1 through TH<sub>m</sub> as shown in figure FIG. 19. It also includes the decreasing coefficients .alpha.1 through .alpha.m ( $1 > .alpha.1 > .alpha.2 \dots .alpha.m > 0$ ) in correspondence with the address management threshold values TH1 through TH<sub>m</sub>.

Detailed Description Text (72):

When the allowed transmission rate is transmitted from the allowed transmission rate calculating unit 52 to the ER write controlling unit 61, and a congestion notification signal is transmitted from the congestion detection controlling unit 54, the ER calculating unit 62 reads a corresponding decreasing coefficient from the ER change parameter table 63 based on an address management threshold value included in the congestion notification signal, and multiplies the allowed transmission rate transmitted from the allowed transmission rate calculating unit 52 by the read decreasing coefficient, in order to obtain the allowed transmission rate. Then, the allowed transmission rate so obtained is written to the ER fields of forward and backward RM cells, and these cells are transmitted.

Detailed Description Text (92):

Also a rate changing unit 207 particularly relates to the present invention, and is

arranged in a backward channel directed from the demultiplexer 205 to the subscriber line processing device 203. It calculates the explicit rate ER based on both the allowed transmission rate  $Ba(n)$  calculated by the rate calculating unit 206, and the number of times that the switching unit 201 sets the EFCI bit in a user data cell passing along that channel, and writes the calculated explicit rate ER to an RM cell.

Detailed Description Text (95):

To overcome this problem, a capability for setting an EFCI bit in a header of a user data cell depending on an internal congested state, is arranged in the switching unit 201 of the system shown in FIG. 21. Additionally, a rate changing unit 207, to be described later, is arranged in a backward (downward) channel directed from the demultiplexer 205 to the subscriber line processing device 203. The rate changing unit 207 measures the setting ratio of the EFCI bit for a user data cell passing along the backward channel, calculates the explicit rate ER based on the result of the measurement and the allowed transmission rate  $Ba(n)$  calculated by a rate calculating unit 206, which will be described later, and writes this rate to an RM cell passing along the backward channel. With such a configuration, an occurrence of congestion in the switching unit 201 can be suppressed.

Detailed Description Text (106):

The congestion detecting unit 403 detects existence/non-existence of congestion (or congestion level) of each subscriber line, by making a comparison between the number of addresses stored in each of the address management buffers 402 corresponding to each subscriber line, and a predetermined threshold value (or a plurality of threshold values), for each subscriber line. Here, the number of addresses stored in each of the address management buffers 402 indicates that cells, the number of which is equal to the number of addresses, remain in the shared buffer memory 401, for a subscriber line corresponding to the address management buffer 402. Accordingly, the congested state of each subscriber line can be detected by monitoring each of the numbers of addresses. The congestion detecting unit 403 then notifies the existence/non-existence of congestion (or congestion level) to the ER writing unit 404, for each subscriber line.

Detailed Description Text (107):

The rate calculating unit 206 (also refer to FIG. 21) counts the number of active virtual connections (VCs) for each subscriber line, and calculates the allowed transmission rate  $Ba(n)$  which is a transmission rate equally assigned to each VC as a result of dividing the transmission rate of each subscriber line by each number of active VCs. The rate calculating unit 206 notifies the allowed transmission rate  $Ba(n)$  for each subscriber line of the ER writing unit 404 and the rate changing unit 207 (refer to FIG. 21) to be described later.

Detailed Description Text (111):

The allowed transmission rate calculating unit 504 calculates the allowed transmission rate  $Ba(n)$  which is a transmission rate equally assigned to each VC, as a result of dividing a transmission rate of each subscriber line (normally the same rate) by the value of the active VC number storing counter 503, for each subscriber line. The rate calculating unit 206 notifies the allowed transmission rate  $Ba(n)$  of each subscriber line, to the ER writing unit 404 and the rate changing unit 207, to be described later (refer to FIGS. 21 and 27).

Detailed Description Text (112):

In FIG. 24, the allowed transmission rate  $Ba(n)$  of each subscriber line notified from the rate calculating unit 206 is assigned to the ER field (described later in FIG. 26) of an RM cell, when the RM cell of each subscriber line is read from the shared buffer memory 401. Otherwise, the ER writing unit 404 may change the allowed transmission rate  $Ba(n)$  based on existence/non-existence of congestion (or a congestion level) of each subscriber line, which is notified from the congestion detecting unit 403, and assign this rate to the RM cell, without assigning the

unchanged notified allowed transmission rate  $Ba(n)$ . The congested state of the demultiplexer 205 is reflected on the changed allowed transmission rate  $Ba(n)$ , in this case. In this way, an RM cell of each subscriber line, to which the allowed transmission rate  $Ba(n)$  is assigned, is transferred to each rate changing unit 207, which is arranged in each backward channel directed from the demultiplexer 205 to each subscriber line processing device 203. Then, the explicit rate ER on which the congested state of the switching unit 201 is reflected, is assigned to that RM cell.

Detailed Description Text (124):

The ER writing unit 605 calculates the explicit rate ER by dividing the allowed transmission rate  $Ba(n)$  assigned to the ER field of the RM cell by the divisor value notified from the ER changing unit 604, when the RM cell is transferred from the demultiplexer 205. It then assigns the calculated explicit rate ER to the ER field of that RM cell, and transmits the RM cell to the subscriber line processing device 203.

Detailed Description Text (126):

FIG. 28 exemplifies a relationship between the degree of congestion  $C(n)$  in a current observation period, and a predetermined threshold value, between which the ER changing unit 604 makes a comparison, and a relationship between the degree of congestion  $C(n)$ , the predetermined threshold value, and the dividing process performed in the ER writing unit 605.

Detailed Description Text (128):

The ER changing unit 604 sets the divisor value "1" while  $C(n)$  does not exceed the threshold value (1) (in a period A). In this case, congestion does not occur in the switching unit 201. Accordingly, the ER writing unit 605 assigns the allowed transmission rate  $Ba(n)$  as the explicit rate ER as it is.

Detailed Description Text (129):

If  $C(n)$  exceeds a threshold value  $S(1)$  (period B), the ER changing unit 604 sets a divisor value 2. The switching unit 201 becomes lightly congested in this case. The ER writing unit 605 sets a value obtained by dividing the allowed transmission rate  $Ba(n)$  by the value (2), as the explicit rate ER.

Detailed Description Text (130):

If  $C(n)$  exceeds also the threshold value  $S(2)$  (period C), The ER changing unit 604 sets a divisor value "4". In this case, the switching unit 201 becomes heavily congested. Then, the ER writing unit 605 sets the value obtained by dividing the allowed transmission rate  $Ba(n)$  by the value "4", as the explicit rate ER.

Detailed Description Text (138):

If congestion occurs in a first SRM in the switching unit 201 when a cell whose ER is set to 150 Mbits/s passes through the switching unit 201, the EFCI bit of that cell is set to "1" in order to notify the congestion, as shown in this figure. If the ER changing unit 604 sets a divisor value, for example, as "2", for this congestion according to the above described method, the ER writing unit 605 assigns the value obtained by dividing the explicit rate ER by 2, that is, 75 Mbits/s, to the cell as a new ER.

Detailed Description Text (142):

The switching unit 201' in the ATM switching system comprises a plurality of SRMs in a similar manner as in the switching unit shown in FIG. 21. The rate calculating unit shown in FIG. 25 is arranged for each of the SRMs. Each of the rate calculating units 206 calculates the allowed transmission rate  $Ba(n)$  based on a congested state in a corresponding SRM, according to the above described method. The calculated allowed transmission rate  $Ba(n)$  is transmitted to the ER writing unit 404, which may be arranged for each of the SRMs in order to correspond to the rate calculating unit 206 of each of the SRMs. Furthermore, the rate changing unit

207 shown in FIG. 21 may be arranged for each of the SRMs. For example, a new ER value is assigned to the ER field of a cell each time the cell passes through an SRM, as shown in FIG. 31, in this case.

Detailed Description Text (170):

When receiving a cell from a transmitting terminal, the cell extracting unit 701 outputs a cell detection signal indicating that the cell is detected, to the communicating connection number counting unit 702, extracts a connection identifier from that cell, and outputs the extracted identifier to the communicating connection number counting unit 702. The communicating connection number counting unit 702 counts the number of communicating connections according to the method of the present invention, and outputs the result to the explicit rate ER calculating unit 703 (ER controlling unit). The explicit rate ER calculating unit 703 calculates the ER based on the counted number of communicating connections, and writes the result to that cell.

CLAIMS:

8. A controlling system for notifying an allowed transmission rate to a terminal in an ATM network, comprising: a memory for temporarily storing cells transmitted from a transmitting terminal; allowed transmission rate calculating means for calculating the allowed transmission rate in correspondence with an output channel; an address management memory for managing addresses of cells stored in said memory; congestion detection controlling means for detecting congestion based on one of an amount of storage of said address management memory and an amount of storage of said memory; and assigning means for writing one of the allowed transmission rate received from said allowed transmission rate calculating means, and a value obtained by lowering the allowed transmission rate according to a congestion notification signal received from said congestion detection controlling means, to a control cell, in order to notify the allowed transmission rate to the terminal, wherein said allowed transmission rate calculating means obtains a number of active connections in which more than one cells arrive during an observation period, in correspondence with an output channel, and calculates the allowed transmission rate by dividing a band of the output channel by the obtained number.

9. The controlling system according to claim 8, wherein said allowed transmission rate calculating means comprises: an arrived cell number counter for counting a number of arrived cells in correspondence with the output channel, and defining a time point at which the counted number reaches a predetermined number, as a termination of the observation period; an active table to which a connection identifier of an arrived cell, which corresponds to the output channel, is written; an active number counter for counting the connection identifier, which corresponds to the output channel, and is written to the active table, and obtaining a number of active connections; and allowed transmission rate calculation controlling means for calculating the allowed transmission rate by dividing the band of the output channel by the number of active connections counted by said active number counter in correspondence with the output channel for which said arrived cell number counter counts the predetermined number.

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L7: Entry 42 of 196

File: USPT

Sep 11, 2001

DOCUMENT-IDENTIFIER: US 6289397 B1

TITLE: Disk drive or like peripheral storage device adapted for firmware upgrading, self-testing, etc.

Abstract Text (1):

A flexible magnetic disk drive is disclosed which is linked to a computer via a universal serial bus interface having firmware held on a read-only memory. In order to facilitate the upgrading of the firmware, an electrically erasable, programmable ROM is employed for firmware storage. Each new firmware version is issued in the form of a flexible magnetic disk which may be loaded in the disk drive just like an ordinary data disk, only with the disk drive disconnected from the computer as far as data transmission is concerned. The EEPROM is preprogrammed to identify the loaded firmware disk, erase the old firmware version on the ROM, and write the new version thereon. In another embodiment a self-testing program disk is employed in place of the firmware disk, for performing a set of tests on the disk drive including the interface. The tests are conducted automatically as the self-testing program disk is loaded in the disk drive, again with the disk drive disconnected from the computer.

Application Filing Date (1):

19990604

Brief Summary Text (8):

The first described method involves the trouble of sending the complete peripheral to the manufacturer or to the authorized service shop at the costs of considerable time, labor and expense. Although this trouble is absent from the second method, reprogramming by the user himself is no easy task, with a high likelihood of write errors being introduced into the firmware, potentially seriously affecting the performance of the peripheral or of the complete computer system.

Brief Summary Text (13):

Most broadly, the invention may be summarized as a data storage device to be connected to a computer via connector means, for interchangeable use with a first kind of storage medium for storing data used by the computer and a second kind of storage medium storing data not used by the computer. The data storage device comprises: (a) data transfer means for data transfer with the first or the second kind of storage medium as these media are interchangeably loaded in the data storage device, the data transfer means being capable of at least reading the first or the second kind of storage medium; (b) means for determining whether or not the data storage device is connected to the computer in terms of data transmission, in order to permit the data storage device to operate under the control of the computer when the data storage device is determined to be connected to the computer; (c) means for identifying the storage medium loaded in the data storage device; and (d) means for causing the data transfer means to read the loaded storage medium when the data storage device is determined to be not connected to the computer and, at the same time, when the loaded storage medium is identified as being of the second kind.

Brief Summary Text (15):

Thus, stated in another aspect thereof, the present invention concerns a data

storage device, to be interfaced with a computer, for interchangeable use with a data storage medium and a firmware storage medium, the latter holding a new version of interfacing firmware. The device comprises: (a) interface means including an erasable, programmable memory on which is stored an old version of interfacing firmware; (b) means for determining whether or not the data storage device is connected to the computer in terms of data transmission, in order to permit the data transfer means to make data transfer with the data storage medium under the control of the computer when the data storage device is determined to be connected to the computer; (c) means for identifying the loaded storage medium as a firmware storage medium when the data storage device is determined to be not connected to the computer; and (d) means for replacing the old firmware version on the memory of the interface means by the new version on the firmware storage medium when the data storage device is determined to be not connected to the computer and, at the same time, when the loaded storage medium is identified as a firm-ware storage medium.

Detailed Description Text (5):

The FDD 5 is shown divided into a data storage section 6 and an interface section 7. For data transfer with a replaceable, double-sided flexible magnetic disk 8, the data storage section 6 is shown to conventionally comprise an electric disk drive motor 9 for imparting rotation to the disk, a motor driver circuit 10 for controllably driving the motor, a pair of transducers or magnetic heads 11 and 12 for reading and writing data on the opposite sides of the disk, a carriage 13 carrying the transducers, a stepper motor 14 controllably driven by a driver circuit 15 and coupled to the transducer carriage 13 via a motion translating mechanism such as a lead screw 16 for moving the transducers across the tracks on the disk and positioning them on any desired track position, a read/write circuit 17 connected to both transducers, an optoelectronic Track Zero sensor 18, and a control circuit 19 for controlling the motor driver circuits 10 and 15 and the read/write circuit 17.

Detailed Description Text (6):

Inserted into the FDD 5, the disk 8 is loaded on a turntable 9a mounted fast to a spindle which is shown coupled directly to the disk drive motor 9 for joint rotation therewith. The disk is to rotate at 300 or 360 revolutions per minute during reading or writing. Connected between disk drive motor 9 and control circuit 19, the motor driver circuit 10 sets the motor into rotation in response to a MOTOR ON signal from the control circuit.

Detailed Description Text (8):

Connected between both transducers 11 and 12 and the control circuit 19, the read/write circuit 17 includes means for processing data read from the disk 8, and means for processing data to be written. The processed read data is sent to the control circuit 19, and the write data is received therefrom.

Detailed Description Text (10):

The control circuit 19 is connected to the FDD interface section 7 for inputting therefrom a MOTOR ON signal Mon, a DRIVE SELECT signal Ds, stepping pulses Sp, a stepping direction signal Dr, and write data Wd over lines 20, 21, 22, 23 and 24, respectively. In response to these input signals the control circuit 19 controls the various parts of the FDD data storage section 6 in order to cause the write data WD to be written on the disk and the data on the disk to be read. Further the control circuit 19 sends the read data Rd and Track Zero signal Too to the FDD interface section 7 by way of lines 25 and 26, respectively. Actually, there are many more standard signal lines between data storage section 6 and interface section 7 of the FDD 5 but are not shown because of impertinence to the instant invention.

Detailed Description Text (12):

Typically, the FDD interface section 7 may take the form of an interface board, having an FDD controller 28, a USB interface 29, and a supply circuit 30 mounted on

a printed circuit board. The USB interface 29 is connected by way of a line 33 to a connector 31 to which there is detachably coupled the noted connector 4b on one end of the USB cable 4 leading to the USB hub 3. The line 33 is understood to represent two signal lines connected respectively to the two signal lines of the USB cable 4.

Detailed Description Text (15):

Itself well known in the disk drive art, the FDD controller 28 puts out the noted MOTOR ON signal Mon. DRIVE SELECT signal Ds, stepping pulses Sp, stepping direction signal Dr, and write data Wd, for delivery to the control circuit 19 of the FDD data storage section 6 over the lines 20-24, and inputs the read data Rd and Track Zero signal Too from the FDD data storage section over the lines 25 and 26. The FDD controller 28 has a supply terminal 28a connected to the five-volt supply line 34.

Detailed Description Text (23):

With reference back to FIG. 1 the supply circuit 30 has an input connected to the five-volt supply line 34 and has a 3.3-volt output line 41, 4.3-volt output line 51, and 5.0-volt output line 52. The 3.3-volt output line 41 is connected to the supply terminal 40 of the USB interface 29. The 4.3-volt output line 51 is connected to the supply terminal 15a of the stepper motor driver circuit 15. The 5.0-volt output line 52 is connected to all of the supply terminal 10a of the disk drive motor driver circuit 10, the supply terminal 17a of the read/write circuit 17, and the supply terminal 19a of the control circuit 19. The voltage applied to the stepper motor 14 is made lower than that to the disk drive motor 9 in order to realize low current energization of the disk drive motor. It is understood that the supply circuit 30 is conventionally furnished with switches, not shown, for on/off control of power fed over the output lines 51 and 52 in order to avoid the concurrent application of starting currents to both motors 9 and 14.

Detailed Description Text (24):

Preferably, and as indicated at 53 in FIG. 1, the FDD 5 is provided with a pilot lamp, which in practice may take the form of a light emitting diode connected to the control circuit 19, for visually indicating the fact that the disk 8 is being accessed. Additionally, according to the present invention, the pilot lamp 53 is also to glow when new firmware is being written on the EEPROM 44, FIG. 2, of the USB interface 29 in a manner to be detailed subsequently. The pilot lamp 53 may be made to blink upon completion of firmware writing, informing the user of that fact.

Detailed Description Text (28):

The FDD 5 may be connected to the computer 1 via the USB cables 2 and 4 and USB hub 3, just as shown in FIG. 1, in use of the FDD as external data storage of the computer. With the data disk 1 loaded on the turntable, the power switch 34b may be closed for setting the disk drive motor 9 into rotation. Computer data will be written on, and read from, the data disk 1 by the transducers 11 and 12 in the usual manner.

Detailed Description Text (34):

It is then questioned at S.sub.7 whether the FDD 5 is ready for reading and writing, that is, whether a disk is loaded on the turntable 9a and, at the same time, the transducers 11 and 12 positioned on Track Zero. The FDD 5 is understood to include a disk sensor, not shown, for informing the control circuit 19 of the loading of the disk 8 or 8a on the turntable 9a. The Track Zero sensor, capable of optically sensing the positioning of the transducers 11 and 12 on Track Zero on the loaded disk, is shown at 18 in FIG. 1. The standard practice in the disk drive art is automatically to position the transducers on Track Zero when the FDD is powered on, as by the closure of the power switch 34b; under the direction of the FDD control circuit 19, notably, its recalibration means 27.

Detailed Description Text (37):

Upon agreement of the recovered self-identifying data with that of the current firmware on the ROM 44, the desired new firmware is read out from the firmware disk at S.sub.190 for temporary storage on the RAM 45, FIG. 2. Further, at this same step S.sub.10, the old firmware is erased from the USB interface EEPROM location 49, and the new firmware is written in its stead. Then the program comes to an end at S.sub.11.

Detailed Description Text (45):

The self-testing startup program is the one needed for automatically starting the FDD and making it ready for self-testing by the program written on the self-testing disk. Read out from the EEPROM 44 when the FDD is powered on, the self-testing startup program is held on the RAM 45 preparatory to execution.

Detailed Description Text (46):

As indicated in FIG. 9, the self-testing disk 8b has a region a where self-identification data is written, a region A.sub.32 where the self-testing program is written, and a blank A.sub.33 where the results of the tests are to be recorded after the execution of the self-testing program. The self-identification data is that which identifies the self-testing disk as such. The self-testing program on the disk region A.sub.32 may include tests on the following interface components and FDD operations:

Detailed Description Text (50):

Reading from specific addresses of the ROM 44 and RAM 45, and writing on the RAM as well.

Detailed Description Text (54):

The self-testing disk is actually formatted, and the results evaluated. The disk formatting requires all the information that has been recorded on the disk to be transferred to the RAM 45 beforehand.

Detailed Description Text (55):

5. Reading and writing:

Detailed Description Text (56):

The first and the last blocks of the disk are tested by writing and reading data thereon.

Detailed Description Text (59):

Reference is now directed to FIG. 10 in which is flowcharted the self-testing startup program. At S.sub.10 in this flowchart is indicated the startup routine which is equivalent to steps S.sub.1 -S.sub.8 of the firmware upgrading program in FIGS. 5 and 6. Therefore, at the end of this startup routine, the self-identifying data of the self-testing disk is understood to have been read on the location A.sub.31, FIG. 9, of the disk. If the loaded disk proves to be a self-testing disk at the next step S.sub.21, then at S.sub.22 the whole data that has been written on this disk is transferred to and stored on the RAM 45, FIG. 8 of the USB interface 29a on a temporary basis.

Detailed Description Text (60):

Then the above listed tests are conducted at S.sub.23 according to the self-testing program now being held on the RAM 45. The next step S.sub.24 dictates the retransfer of the whole data from RAM 45 to disk 8b, together with the results of the tests, which are recorded as aforesaid on the blank A.sub.33 as of the disk. The program ends at S.sub.24.

Detailed Description Text (64):

2. Upon completion of firmware rewriting, a log file may be opened on the firmware disk for recording the fact.

## CLAIMS:

1. A data storage device to be connected to a computer via connector means, for interchangeable use with a first kind of storage medium for storing data used by the computer and a second kind of storage medium storing data not used by the computer, the data storage device comprising:

(a) data transfer means for data transfer with the first or the second kind of storage medium as these media are interchangeably loaded in the data storage device, the data transfer means being capable of at least reading the first or the second kind of storage medium;

(b) means for determining whether or not the data storage device is connected to the computer in terms of data transmission, in order to permit the data storage device to operate under the control of the computer when the data storage device is determined to be connected to the computer;

(c) means for identifying the storage medium loaded in the data storage device; and

(d) means for causing the data transfer means to read the loaded storage medium when the data storage device is determined to be not connected to the computer and, at the same time, when the loaded storage medium is identified as being of the second kind.

4. A data storage device to be connected to a computer via connector means, for interchangeable use with a data storage medium and one or more prescribed software storage media, the data storage device comprising:

(a) data transfer means for data transfer with a data storage medium or a software storage medium as these media are interchangeably loaded in the data storage device, the data transfer means being capable of at least reading the data storage medium or the software storage medium;

(b) means for determining whether or not the data storage device is connected to the computer in terms of data transmission, in order to permit the data transfer means- to make data transfer with the data storage medium under the control of the computer when the data storage device is determined to be connected to the computer;

(c) means for identifying the loaded storage medium when the data storage device is determined to be not connected to the computer; and

(d) means for causing the data transfer means to read the loaded storage medium when the data storage device is determined to be not connected to the computer and, at the same time, when the loaded storage medium is identified as a prescribed software storage medium.

5. A data storage device to be connected to a computer via connector means, for interchangeable use with a data storage medium and a firmware storage medium, the latter holding a new version of interfacing firmware, the data storage device comprising:

(a) data transfer means for data transfer with a data storage medium or a firmware storage medium as these media are interchangeably loaded in the data storage device, the data transfer means being capable of at least reading the data storage medium or the firmware storage medium;

(b) interface means including an erasable, programmable memory on which is stored an old version of interfacing firmware for adapting the data storage device to the

computer;

(c) means for determining whether or not the data storage device is connected to the computer in terms of data transmission, in order to permit the data transfer means to make data transfer with the data storage medium under the control of the computer when the data storage device is determined to be connected to the computer;

(d) means for identifying the loaded storage medium as a firmware storage medium when the data storage device is determined to be not connected to the computer; and

(e) means for replacing the old firmware version on the memory of the interface means by the new version on the firmware storage medium when the data storage device is determined to be not connected to the computer and, at the same time, when the loaded storage medium is identified as a firmware storage medium.

6. A data storage device to be connected to a computer via connector means, for interchangeable use with a data storage medium and a self-testing program storage medium, the latter medium having prewritten thereon a set of tests to be conducted on the data storage device, the data storage device comprising:

(a) data transfer means for data transfer with a data storage medium or a self-testing program storage medium as these media are interchangeably loaded in the data storage device;

(b) means for determining whether or not the data storage device is connected to the computer in terms of data transmission, in order to permit the data transfer means to make data transfer with the data storage medium under the control of the computer when the data storage device is determined to be connected to the computer;

(c) means for identifying the loaded storage medium as a self-testing program storage medium when the data storage device is determined to be not connected to the computer; and

(d) means for performing the set of tests according to the program on the self-testing program storage medium when the data storage device is determined to be not connected to the computer and, at the same time, when the loaded storage medium is identified as a self-testing program storage medium.

11. The method of claim 10 wherein the currently loaded storage medium is identified by reading self-identification data written in a prescribed location on the storage medium.

13. The method of claim 12 which further comprises writing, upon completion of the tests, the self-testing program and the results of the tests on the storage medium.

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L7: Entry 168 of 196

File: USPT

Oct 8, 1974

DOCUMENT-IDENTIFIER: US 3840864 A  
TITLE: MULTIPLE MEMORY UNIT CONTROLLER

Abstract Text (1):

A memory control unit for determining the actual physical location of an instruction address in one of a plurality of memory units in a digital computer wherein the instruction address and the memory addresses are both in a block, track and word hierarchy, where the instruction address may not correspond to the memory address due to differences in the number of available blocks for recording program instructions from memory unit to memory unit, utilizing: a block address register for storing the block portion of the instruction address; a shift register associated with each memory unit wherein the number of available blocks for each memory unit is stored; a flip flop for bit by bit comparison of the contents of the block address register with the contents of selected shift registers; a counter for shifting from one to another of the shift registers when the contents of the block register exceeds the contents of the selected shift register, and an adder for decrementing the contents of the block address register by an amount equal to the number contained in the previously selected shift register. The memory control unit also includes another flip flop responding to the bit by bit serial comparison of the block address register and the selected shift register for detecting whether the instruction address starts in the last available block in a memory unit, and a circuit for evaluating the track and word portion of the address of each word of the instruction being executed for determining when the last word of an instruction has been executed by the computer.

Application Filing Date (1):  
19740114

Brief Summary Text (7):

By solving these problems, it would be possible to write programs for a particular class of computers without regard to the actual physical memory combination of each individual computer system; thereby making it economic to write a library of programs for the class as a whole.

Detailed Description Text (3):

Referring to the Figures by the characters of reference, there is illustrated in FIG. 1 a plurality of memory units 10, 12, 14 and 16 operatively coupled through a memory control unit 18 to a central processor 20 of a computer. The first memory unit 10, labeled zero, represents the memory unit which may be physically located in a central processing unit of a computer. An example of such a computer having this type of disc memory is disclosed in U.S. Pat. No. 3,579,192 entitled Data Processing Machine, which is assigned to the same assignee. The other three memory units 12, 14 and 16, labeled one, two and three, are used as supplementary memories in order to expand the memory capacity of the computer. In the system of FIG. 1, it is a desirable feature that the central processing unit 20 be able to operate with memory units 10, 12, 14 and 16 each having a different number of available blocks. Additionally, it is a desirable feature of the system of FIG. 1 that a program be operable with the central processing unit regardless of the number of memory units of the system and the number of available blocks on each individual memory unit. Naturally, the length of a program must not exceed the total number of available

blocks on the system. It is, therefore, one of the ultimate objectives of this invention to make the physical boundaries of each memory unit transparent to any program executed by central processing unit 20. As will hereinafter become apparent, each of the supplementing memory units 12, 14 and 16 may be added to or removed from the system without the necessity of making changes to the program or instruction addresses. It should be remembered, however, that if the number of available blocks in any memory unit is changed, or a memory unit is removed or added, it is of course necessary to reload the program, i.e., to write the program instruction on to the revised memory unit structure and to record the new number of available blocks in the memory control unit shift registers as discussed in connection with FIG. 8.

Detailed Description Text (48):

The memory control unit 18, as previously indicated receives its timing from the central processing unit 20 and also from the central processing unit 20 and also from the selected memory units 10, 12, 14 or 16, as is commonly done in the art, in order to process the information between the central processing unit 20 and the selected memory unit. The timing from the memory units 10, 12, 14 and 16 is received from the timing track on the memory units. Once the memory control unit 18 has selected the appropriate memory unit, data transmission between the central processing unit 20 and the selected memory unit begins. In response to the above, and in cooperation with the several individual units in the memory control unit 18, the memory control unit will automatically switch from memory unit to memory unit when during the execution of an instruction by the computer the length of the instruction exceeds the number of available blocks on the first selected memory unit.